ABSTRACT

[0053] A process and apparatus directed to forming metal plugs in a peripheral logic circuitry area of a semiconductor device to contact both N+ and P+ doped regions of transistors in the peripheral logic circuitry area. The metal plugs are formed after all high temperature processing used in wafer fabrication is completed. The metal plugs are formed without metal diffusing into the active areas of the substrate. The metal plugs may form an oval slot as seen from a top down view of the semiconductor device.